REMARKS

In response to the Office Action mailed on <u>August 5, 2003</u>, claims 32 and 40 are amended; as a result, claims <u>13-16 and 32-60</u> are now pending in this application.

This paper incorporates all of the previous arguments used in addressing the rejections. Applicant reserves the right to use the arguments in an appeal of the present application if appropriate.

§103 Rejection of the Claims

Claims 13-16 and 32-60 were rejected under 35 USC § 103(a) as being unpatentable over Katayama et al. (U.S. Patent No. 5,875,452) in view of Rosich et al. (U.S. Patent No. 5,587,964). Applicant respectfully traverses the rejections. Grounds for the traversal for the individual claims are stated below.

Regarding claim 13:

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

First, Applicant is unable to find in the cited portions of the proposed combination of references, among other things, a unidirectional command and address bus coupled to the memory controller and a bidirectional data bus coupled to the memory controller, as recited in claim 1. Katayama shows a single bus for address and data (*see* FIG. 9 of Katayama) and Rosich does not show a bidirectional data bus coupled to a memory controller (*see* FIG. 5 of Rosich).

Second, Applicant cannot find, a plurality of N memory modules, wherein each of the memory modules includes a second data register connected between the plurality of memory devices and the bidirectional data bus, as recited in part in claim 13. This element of claim 13 results in "N" data registers. Applicant is unable to find a number of data register that varies with a quantity "N" in the proposed combination of references.

Third, Applicant cannot find, wherein a first load on the command and address bus is equal to N devices and a second load on the data bus is equal to N devices where the total number of memory devices is N*M. Instead, the load on the refresh counter register in

Katayama would be the total number of memory devices (Ref. 22 in FIG. 9 of Katayama). Because the present application organizes the memory into N subsystems of M memory devices, the command register and the data register in the memory controller do not have to drive the total number (N*M) of devices as do registers referred to in Katayama or Rosich. Therefore, the load is reduced in comparison to the approach in Katayama or Rosich.

The Office Action cites *St. Regis Paper Co. v Bemis Co.* in noting that to duplicate parts for multiple effects is not given patentable weight. *See* Office Action page 5. However, an assertion that the present application is a mere duplication of parts over the prior art is a mischaracterization of the present application because the present application goes much further. The present application provides an architecture that is a different than the prior art. By adding modules, the present application adds memory subsystems, not merely adding memory devices. The reorganization into subsystems provides, among other things, the reduced loading discussed above. Because of these differences and their advantages, Applicant respectfully submits that the present application is not a mere duplication of parts.

Applicant respectfully requests reconsideration and allowance of claim 13.

Regarding claims 14 – 16:

If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596(Fed. Cir. 1988).

Claims 14-16 depend on claim 13 and are believed to be allowable at least for the reasons stated previously for claim 13.

Applicant respectfully requests reconsideration and allowance of claims 14-16.

Regarding claims 32 and 33:

Claim 32 was amended. Support for the amendment is found generally within the specification. *See e.g.*, FIG. 1. Insofar as the rejection is applied to the amended claim, applicant traverses the rejection. Applicant is unable to find in the cited portions of the proposed combination of references, among other things, a teaching or suggestion of a method including latching the commands and addresses in a first register, latching the data in a data register, driving the latched data to the data in buffers of the memory devices, and storing the data from the data in buffer in the addressable storage of one of the plurality of memory devices, as recited

in claim 32. Instead, Applicant believes the proposed combination of references teach or suggest

a common data in buffer. (*See, e.g.* FIG. 9 of Katayama and FIG. 5 of Rosich.)

Claim 33 depends on claim 32 and is believed to be allowable at least for the reasons

stated previously for claim 32.

Applicant respectfully requests reconsideration and allowance of claims 32 and 33.

Claims 34 and 35:

Applicant is unable to find in the cited portions of the proposed combination of

references, among other things, a teaching or suggestion of a method including latching the

commands and addresses in a first register, driving the latched commands and addresses to a

plurality of memory devices having addressable storage, wherein each memory device includes a

data in and a data out buffer, a column decoder, and a row decoder, communicating data from the

addressable storage of one of the plurality of memory devices, and latching data in the data in

and a data out buffer, as recited in claim 34. Instead, Applicant believes the proposed

combination of references teach or suggest data buffers in common use by the memory devices.

(*See, e.g.* FIG. 9 of Katayama and FIG. 5 of Rosich.)

Claim 35 depends on claim 34 and is believed to be allowable at least for the reasons

stated previously for claim 34.

Applicant respectfully requests reconsideration and allowance of claims 34 and 35.

Claims 36-39:

Applicant is unable to find in the cited portions of the proposed combination of

references, among other things, a teaching or suggestion of a memory module comprising a a

plurality M of memory devices, wherein each memory device internally contains a data in and a

data out buffer, as recited in claim 36. Instead, Applicant believes the proposed combination of

references teach or suggest external data buffers in common use by the memory devices. Claims

37-39 depend on claim 36 and are believed to be allowable at least for the reasons stated

previously for claim 36. Applicant respectfully requests reconsideration and allowance of claims

36-39.

Claims 40 and 41:

Claim 40 was amended. Support for the amendment is found generally within the specification. *See e.g.*, page 11, lines 10 and 11 of the specification. Insofar as the rejection is applied to the amended claim, Applicant respectfully traverses the rejection. Applicant is unable to find in the proposed combination of references, among other things, a teaching or suggestion of a method that includes receiving commands and addresses, through the command and address lines, from the unidirectional command and address bus, the commands and addresses communicated according to a packet protocol and receiving data, through the data lines, from the data bus, the data communicated according to a packet protocol, as recited in claim 40.

Claim 41 depends on claim 40 and is believed to be allowable at least for the reasons stated previously for claim 40.

Applicant respectfully requests reconsideration and allowance of claims 40 and 41.

Regarding claim 42 and 43:

Applicant is unable to find in the cited portions of the proposed combination of references, among other things, a teaching or suggestion of a method including latching the data in a data in and out buffer of the one of the plurality of memory devices and latching the data from the data in and data out buffer in a data register associated with the plurality of memory devices, as recited in claim 42. Instead, Applicant believes the proposed combination of references teach or suggest external data buffers in common use by the memory devices.

Claim 43 depends on claim 42 and is believed to be allowable at least for the reasons stated previously for claim 42.

Applicant respectfully requests reconsideration and allowance of claims 42 and 43.

Claims 44-47, 52-55 and 56-60:

Applicant is unable to find in the cited portions of the proposed combination of references, among other things, a teaching or suggestion of a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer, as recited in claims 44, 52 and 56. Instead, Applicant believes the proposed combination of references teach or suggest external data buffers in common use by the memory devices.

Claims 45-47 depend on base claim 44, claims 53-55 depend on base claim 52 and claims 57-60 depend on base claim 56. Applicant believes claims 45-47, 53-55 and 57-60 are allowable at least for the reasons stated previously for the base claims, namely claims 44, 52 and 56.

Applicant respectfully requests reconsideration and allowance of claims 44 – 47, 52-55, and 56-60.

Claims 48 -51:

Applicant is unable to find in the cited portions of the proposed combination of references, among other things, a teaching or suggestion of a method including driving the latched commands and addresses to the plurality of memory devices having addressable storage, wherein each memory device includes a data in and a data out buffer, a column decoder, and a row decoder, as recited in claims 48 and 50. Instead, Applicant believes the proposed combination of references teaches or suggests external buffers in common use b the memory devices.

Claim 49 depends on base claim 48 and claim 51 depends on base claim 50. Applicant believes that claims 49 and 51 are allowable at least for the reasons stated previously for claims 48 and 50.

Applicant respectfully requests reconsideration and allowance of claims 48-51.

FIG. 6

The Office Action stated that in the amendment filed on July 22, 2002, Applicant admitted on page 1 that the contents of FIG. 6 are believed to contain no new subject matter. The Office Action subsequently states that the statement is an admission of prior art. *See* Office Action page 2. Applicant respectfully submits that the Examiner has misinterpreted the statement.

FIG. 6 was submitted in response to an objection to the drawings made under 37 C.F.R. 1.83(a) in an Office Action mailed March 14, 2002. The objection stated that a drawing was required because "the drawings must show every feature of the invention specified in the claims."

The response to that Office Action date July 15th, 2002 stated "New Fig. 6 is believed supported by the original specification. ... No new matter is believed proposed." Thus, the

statement, correctly interpreted is that FIG. 6 does not propose new subject matter over the

original specification. Applicant respectfully traverses the assertion of prior art in the Office

Action. FIG. 6 was added to overcome an objection and does not introduce new subject matter

over the original specification. The subject matter of FIG. 6 is found generally within the

original specification. *See e.g.*, Page 8 lines 3-13 of the specification.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

KEVIN J. RYAN

By his Representatives,
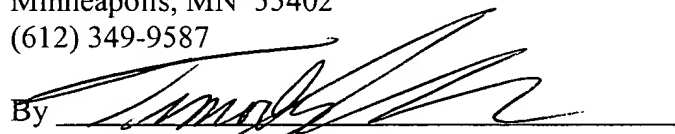
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this ___ day of December, 2003

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